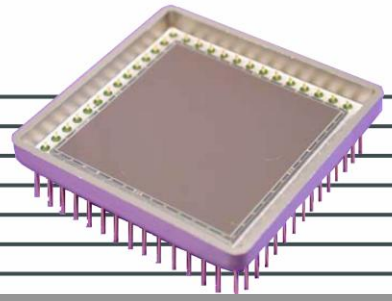
ANDANTA

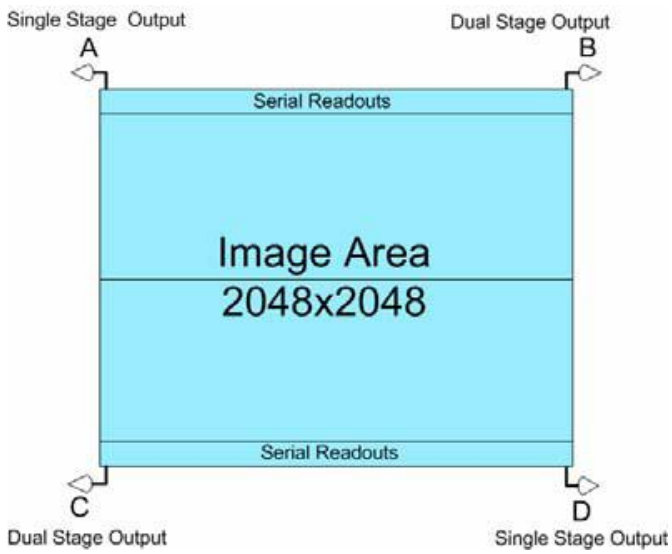


CCD0720A/0820A Image Sensor

2048 x 2048 Element Image Area CCD Image Sensor

Features

- 2048 x 2048 CCD Image Array
- 15 µm x 15 µm Pixel
- 32.2mm x 32.2mm Image Area
- Near 100% Fill Factor
- Readout Noise Less Than 5 Electrons at 150KHz
- 2 Single Stage 5MHz Outputs
- 2 Dual Stage 10MHz Outputs
- Three-Phase Buried Channel NMOS Image area
- Multi-pinned Phase (MPP) option
- Three-Phase Buried Channel Readout Registers
- Selectable Video Output Channels



General Description

The CCD0820A is a 2048 x 2048 image element solid state Charge Coupled Device CCD sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems.

TheCCD0820A is organized in two halves each containing an array of 2048 horizontal by 1024 vertical photosites. The CCD0820A may be operated in either buried-channel or MPP mode. The pixel spacing is 15µm x 15µm. For dark reference, each readout line is preceded by 8 extended pixels. The dual stage output architecture allows higher frame rate operation through two readout sections.

The CCD0820A is offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

Functional Description

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. During integration, the collected photoelectrons are related directly to the amount of charge accumulated at each pixel. There is a linear relationship between the incident illumination intensity and the integration time.

The photosite structure is made up of a series of closely spaced MOS capacitors elements. These photosites sense light, then shift the light vertically via potential wells created by the vertical array clocks.

Vertical Charge Transfer: The charge may be shifted in one of three methods, split frame transfer, single frame transfer to outputs A or B, or single frame transfer to outputs C or D. For low noise performance the charge should be split between outputs A and D, which are the single stage outputs. At the end of an integration period the A1, A2, and A3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout registers. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into a Upper and Lower halves. Each 2048 x 1024 section may be clocked independently or together. Horizontal serial registers along the top and bottom permit simultaneous readout of both halves. The CCD0820 may be clocked such that the full array is readout by the upper or lower serial registers.

Serial, Charge Transfer: S1, S2 and S3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The horizontal serial register is twice the size of the photosite to allow for vertical binning. For both frame transfer configurations, the charge may be read out through the amplifiers at the bottom or top of the image area.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 10 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to the next ordered serial clock for normal full resolution readout.

The reset FET in the horizontal readout, clocked appropriately with RG, allows binning of adjacent pixels.

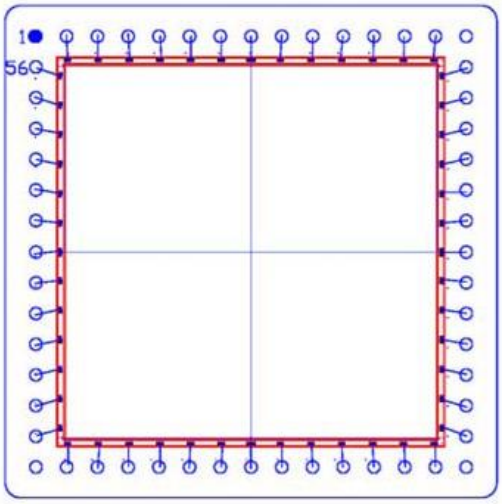
Output Amplifier: The CCD0820 has one output amplifier at the end of each Horizontal register. There are two dual-stage amplifiers with active load FETs that allow for increased data rates. The other two outputs are single stage source followers that have proven low noise performance.

The capacitor is then reset via the reset MOSFET with ϕRG to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning.

The output amplifier drains are tied to OD. The source is connected to an external load resistor to ground and constitutes the video output from the device.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal at the output V_{out} pin is produced.

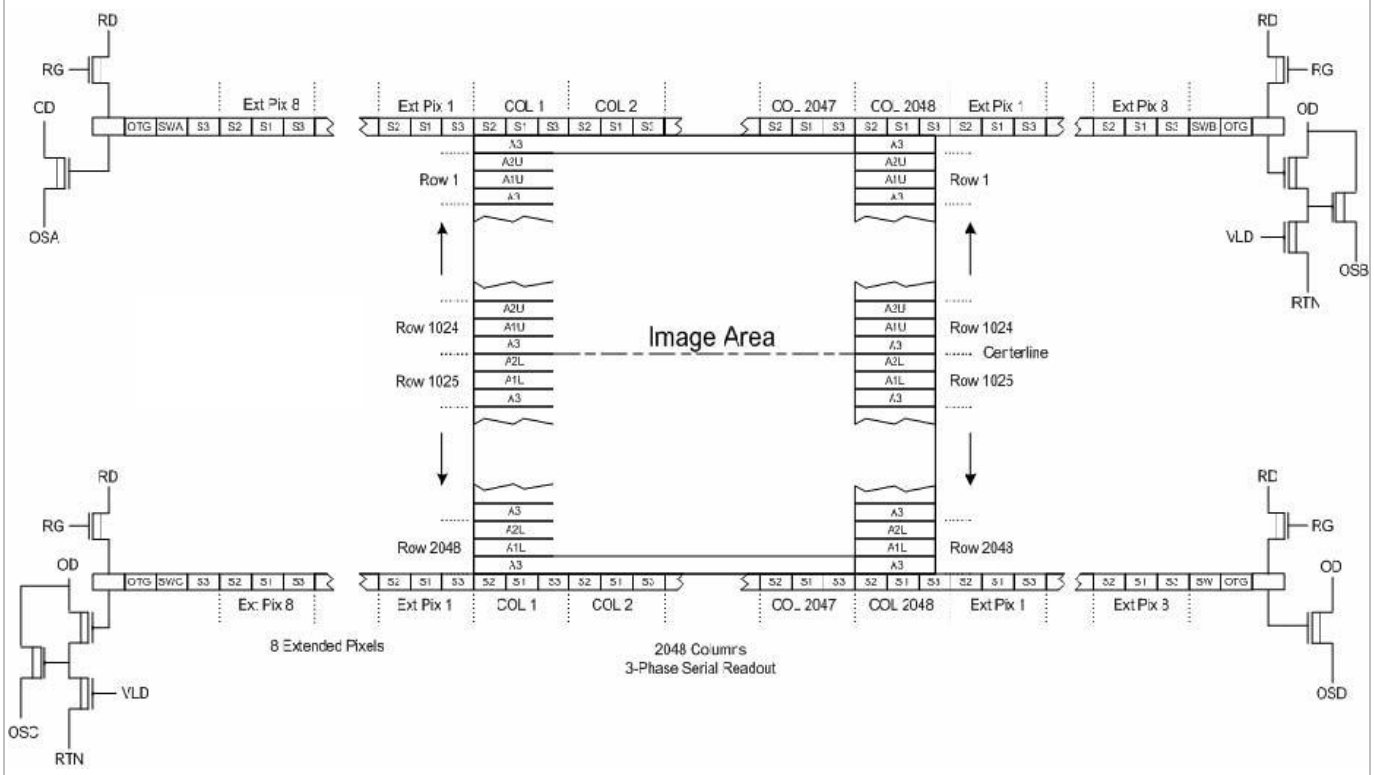
CCD0820A



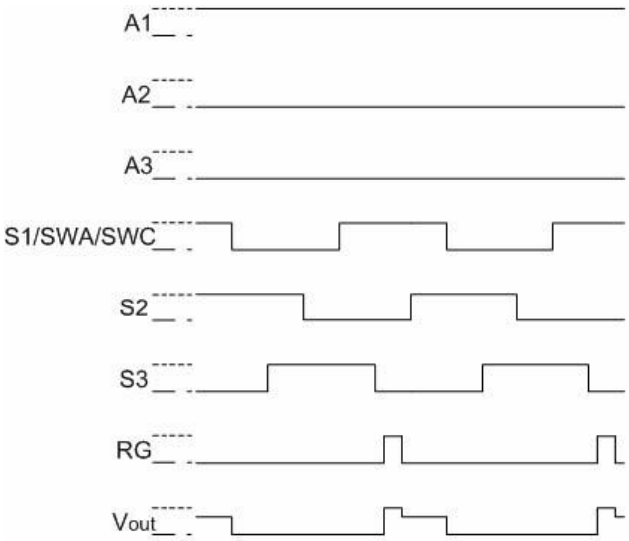
CCD0820A Pin Connections

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	NC	15	NC	29	NC	43	NC
2	RG	16	OSB	30	RG	44	OSC
3	RD	17	VOD	31	RD	45	VOD
4	OTG	18	RTN	32	OTG	46	RTN
5	SWA	19	VLD	33	SWD	47	VLD
6	SUB	20	A1U	34	SUB	48	A1L
7	S2	21	A2U	35	S1	49	A2L
8	S3	22	A3	36	S3	50	A3
9	S1	23	A2L	37	S2	51	A2U
10	NC	24	A1L	38	NC	52	A1U
11	SWB	25	SUB	39	SWC	53	SUB
12	OTG	26	NC	40	OTG	54	NC
13	RD	27	VOD	41	RD	55	VOD
14	RG	28	OSD	42	RG	56	OSA

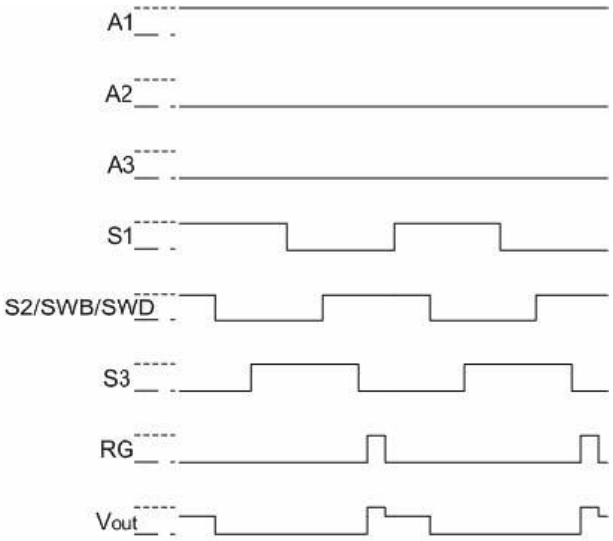
Schematic



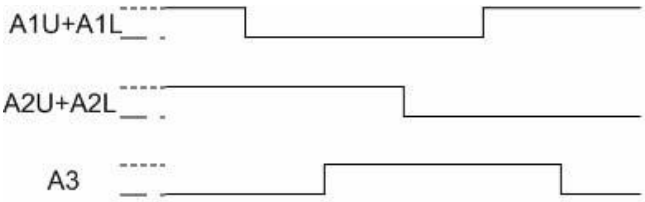
Clock Waveforms



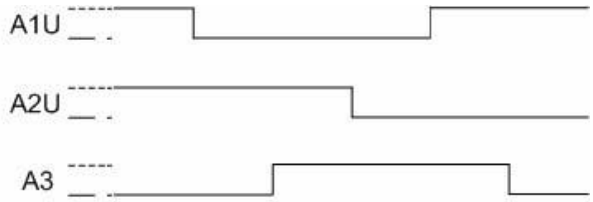
Serial readout 1-2-3 to outputs A and C



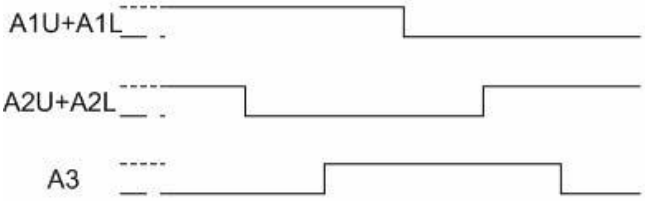
Serial readout 2-1-3 to outputs B and D



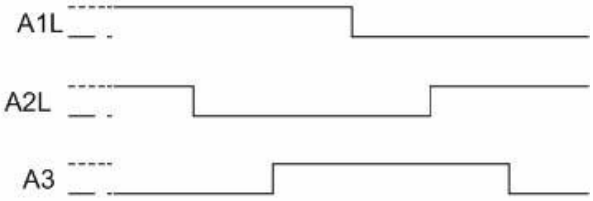
Full Frame Clock up to upper Serial Register 1-2-3



Split Frame Clock up 1-2-3



Full Frame Clock down to lower Serial Register 2-1-3



Split Frame Clock down 2-1-3

DC Operating Characteristics

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
OD	DC Supply Voltage	15.0	24.0	30.0	V	
RD	Reset Drain Voltage	10.0	15.0	20.0	V	
OTG	Output Transfer Gate Voltage	-2.0	-1.0	2.0	V	
Vss	Substrate Ground	0.0			V	
VLD	Dual Stage Output Load Voltage	-5.0	3.0	5.0	V	

Typical Clock Voltages

Symbol	Parameter	High	Low	Unit	Remarks
S1,S2,S3	Horizontal Serial Clocks	+5.0	-5.0	V	Typical clock range
SW	Summing Gate Clock	+5.0	-5.0	V	Clock as S1 or S2 if not clocked separately
A1,A2,A3	Vertical Array Clocks	+4.0	-9.0	V	
Rg	Reset Gate Array Clock	+5.0	-2.0	V	

AC Characteristics

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{ODC}	Output DC Level		14.0		V	Typical
Zsingle	Suggested Load Resistor Outputs A and D	5.0	10.0	20.0	kΩ	Higher resistance reduces bandwidth
Zdual	Suggested Load Resistor Outputs B and C	2.0	5.0	10.0	kΩ	

Performance Specifications

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{SAT}	Saturation Output Voltage Full Well Capacity	600 150k			mV e-	
	Output amplifier sensitivity	5.0			µV/e-	
PRNU	Photo Response Non-Uniformity Peak-to-Peak	10			$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak	1.0			mV	

Cosmetic Grading

Grading and screening of devices establishes a ranking for the image quality that a CCD provides. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighbouring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The CCD0820 CCD image sensor is available in various standard grades, as well as custom grades. Consult ANDANTA GmbH for information on grade selection.

Warranty

ANDANTA GmbH will repair or replace, at our option, any image sensor product within twelve months of delivery to the end customer, for any defect in materials or workmanship. Contact ANDANTA GmbH for further warranty information, a return number, and shipping instructions

Certification

ANDANTA GmbH certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under the performance specifications summarized.

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